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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/722,737	11/28/2000	Kazuhiro Nobori	2000_1645A	5253

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EXAMINER

ROSE, KIESHA L

ART UNIT PAPER NUMBER

2822

DATE MAILED: 01/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/722,737

Applicant(s)

NOBORI ET AL.

Examiner

Kiesha L. Rose

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 October 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 27,29-40 and 56-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 22.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

This Office Action is in response to the RCE and amendment filed 27 October 2003.

Claim Rejections - 35 USC § 112

Claims 27 and 29-40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 27 and 29-40 disclose leading ends of pillared electrodes extending to a uniform height relative to one another. This limitation is not disclosed in the specification, therefore is considered new matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 27-31, 33-35, 38, 40 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (U.S. Patent 5,783,466) in view of Hikita et al. (U.S. Patent 6,133,637) and Juskey et al. (U.S. Patent 6,337,228).

Takahashi discloses a semiconductor device (Figs. 1b and 2c) that contains a first and second semiconductor (12) having electrodes formed on both the upper and lower faces of the semiconductor, a copper heat radiating plate (16) that is joined to the lower face (13) of the semiconductors (12), smooth pressed pillared electrodes (29) that are joined to the heat radiating plate (16) and substantially equally spaced relative to the other, an electric circuit (21) made of copper and set to ceramic with the first and second semiconductor (12) joined thereto, a sealing resin (24,26,27) that covers the first and second semiconductors (12) and a face of the heat radiating plate (16) so that the leading ends of the pillared electrodes (29) are exposed. Takahashi discloses all of the limitations except for the semiconductor chip joined to the heat radiating plate by a conductive paste. Whereas Juskey discloses a semiconductor package (Fig. 5) that contains a semiconductor chip (64), a heat radiating plate (20) and a conductive paste (66) bonded to the lower face of the semiconductor chip to the upper face of the heat radiating plate. The conductive paste is used to thermally connect the chip with the heat radiating plate. (Column 7, lines 34-37) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Takahashi by incorporating a conductive paste to bond together the chip and the heat radiating plate for thermal connection as taught by Juskey. Takahashi and Juskey disclose all of the limitations except for there being pillared electrodes joined to the semiconductors. Whereas Hikita et al discloses a semiconductor device (Figs. 7 and 19) that contains a semiconductor (14) with pillared electrodes (16b) formed on the semiconductor with bump (14c) formed between pillared

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electrodes (16b) and semiconductor (14). The pillared electrodes are formed on the semiconductor to provide an electrical connection to another chip or an external circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor devices of Takahashi and Juskey by incorporating pillared electrodes formed on the semiconductors to provide electrical connections to another chip or an external circuit as taught by Hikita. In regards to Claim 34 referring to the removal of the sealing resin, a "*product by process*" claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972); *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); *In re Fessmann*, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "*product by, all of*" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "*product by process*" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear. "Even though product -by [-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted). Takahashi, Juskey and Hikita disclose the claimed invention except for the leading ends of the pillared electrodes extending to a

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uniform height relative to one another. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the leading ends of the pillared electrodes extending to a uniform height relative to one another, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (1980).

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi, Juskey and Hikita as applied to claim 27 above, and further in view of Sakai et al. (U.S. Patent 5,294,750).

Takahashi, Hikita and Juskey disclose all of the limitations except for the heat radiating plate to contain a ceramic structure with conductor layers therebetween. Whereas Sakai discloses a ceramic package (Fig. 1 and 10) that contains a ceramic heat radiating plate (1) with a ceramic layer (4) with conductor layers (8) formed therebetween. A ceramic heat radiating plate with conductor layers is formed to radiate heat generated in the chip, for high mechanical strength and to have excellent electrical characteristics. (Column 4, lines 24-31) Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor devices of Takahashi, Hikita and Juskey by incorporating a ceramic heat radiating plate with conductor layers to radiate heat generated from the chip, to have high mechanical strength and excellent electrical characteristics as taught by Sakai.

Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al., Hikita and Juskey as applied to claim 28 above, and further in view of Kondoh et al. (U.S. Patent 5,448,114).

Takahashi, Hikita and Juskey disclose all of the limitations except for the pillared electrodes to be formed of materials with different hardnesses and melting points between the inside and outside layers of the electrodes. Whereas Kondoh discloses a semiconductor flip chip (Fig. 19) that contains a pillared electrode that contains a high melting point copper core layer (44) surrounded by a low melting point solder layer (45). The pillared electrode is formed with a core layer surrounded by a solder layer to make the distance between bumps shorter to form narrower pitches. (Column 5, lines 7-10) Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor devices of Takahashi, Hikita and Juskey by incorporating the pillared electrodes to contain materials of different hardnesses and melting points to make distance between bumps shorter to form narrower pitches as taught by Kondoh.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al., Hikita et al and Juskey. as applied to claim 1 above, and further in view of Urushima (U.S. Patent 6,046,495).

Takahashi, Hikita and Juskey disclose all of the limitations except for the heat radiating plate to comprise pits and projections. Whereas Urushima discloses a semiconductor device (Fig. 4a) that contains a heat radiating plate (24) with a heat sink containing pins and projections. The heat radiating plate contains pins and projections to improve heat dissipation. (Column 1, lines 58-60) Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor devices of Takahashi, Hikita and Juskey by incorporating pins and

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projections on the heat radiating plate to improve heat dissipation as taught by Urushima.

Claims 57-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (U.S. Patent 5,783,466) in view of Hikita et al. (U.S. Patent 6,133,637), Juskey et al. (U.S. Patent 6,337,228) and Kondoh et al. (U.S. Patent 5,448,114).

Takahashi discloses a semiconductor device (Figs. 1b and 2c) that contains a first and second semiconductor (12) having electrodes formed on both the upper and lower faces of the semiconductor, a copper heat radiating plate (16) that is joined to the lower face (13) of the semiconductors (12), pillared electrodes (29) that are joined to the heat radiating plate (16) and substantially equally spaced relative to the other, the leading ends of the pillared electrodes (29) are exposed to constitute electric connecting parts. Takahashi discloses all of the limitations except for the semiconductor chip joined to the heat radiating plate by a conductive paste. Whereas Juskey discloses a semiconductor package (Fig. 5) that contains a semiconductor chip (64), a heat radiating plate (20) and a conductive paste (66) bonded to the lower face of the semiconductor chip to the upper face of the heat radiating plate. The conductive paste is used to thermally connect the chip with the heat radiating plate. (Column 7, lines 34-37) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Takahashi by incorporating a conductive paste to bond together the chip and the heat radiating plate for thermal connection as taught by Juskey. Takahashi and Juskey disclose all of the limitations except for there being pillared electrodes joined to the semiconductors.

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Whereas Hikita discloses a semiconductor device (Figs. 7 and 19) that contains a semiconductor (14) with pillared electrodes (16b) formed on the semiconductor with bump (14c) formed between pillared electrodes (16b) and semiconductor (14). The pillared electrodes are formed on the semiconductor to provide an electrical connection to another chip or an external circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor devices of Takahashi and Juskey by incorporating pillared electrodes formed on the semiconductors to provide electrical connections to another chip or an external circuit as taught by Hikita. Takahashi, Hikita and Juskey disclose all of the limitations except for the pillared electrodes to be formed of materials with different hardnesses and melting points between the inside and outside layers of the electrodes. Whereas Kondoh discloses a semiconductor flip chip (Fig. 19) that contains a pillared electrode that contains a high melting point copper core layer (44) surrounded by a low melting point solder layer (45). The pillared electrode is formed with a core layer surrounded by a solder layer to make the distance between bumps shorter to form narrower pitches. (Column 5, lines 7-10) Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor devices of Takahashi, Hikita and Juskey by incorporating the pillared electrodes to contain materials of different hardnesses and melting points to make distance between bumps shorter to form narrower pitches as taught by Kondoh.

Response to Arguments

Applicant's arguments filed 27 October 2003 have been fully considered but they are not persuasive. Applicant's argument in regards to the Takahashi reference not disclosing the lower face of the semiconductor element joined to the heat radiating plate is erroneous. The claimed invention has the heat radiating plate comprising a ceramic and an electric circuit and the Takahashi reference discloses a heat radiating plate comprising a ceramic layer and a copper layer (electric circuit layer) which together also form a heat radiating plate. The lower face of the semiconductor element is joined to the heat radiating plate since the ceramic and copper layer form the heat radiating plate. In addition the claimed invention as shown in fig. 6 is not directly connected to the heat radiating plate but is joined to the electric circuit. Therefore the Takahashi reference does disclose the lower face of the semiconductor element joined to the heat radiating plate, so the rejection stands. In regards to the leading ends of the pillared electrodes extending to a uniform height relative to one another there is no criticality for them being a certain height stated in the specification.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shimizu et al discloses a semiconductor package with a heat radiating plate and semiconductor elements with pillar electrodes joined to the semiconductor elements and heat radiating plate.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


KLR

